EtherNet/IP™ to the Edge – A Concept for "Low-complexity Ethernet"

Tom Weingartner
Analog Devices, Inc.

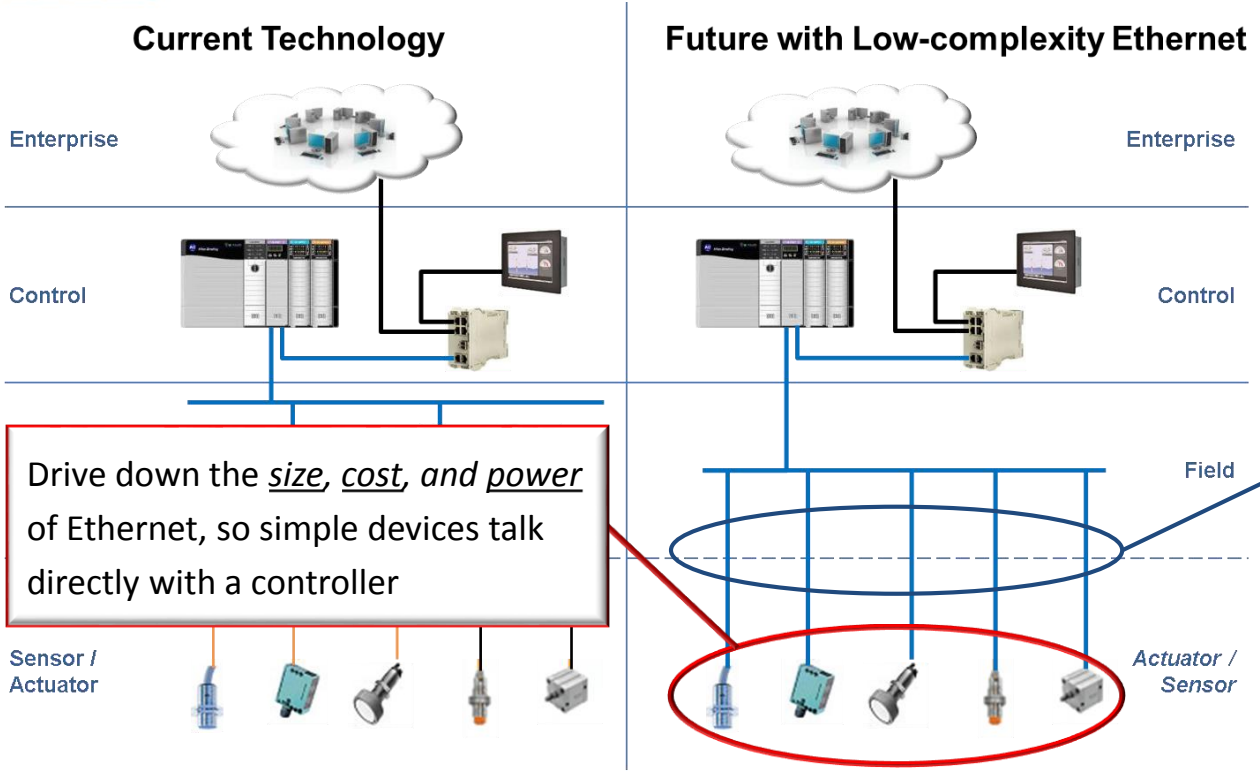
Dave Alsup
Analog Device, Inc.

February 22, 2017

Discussion Topics

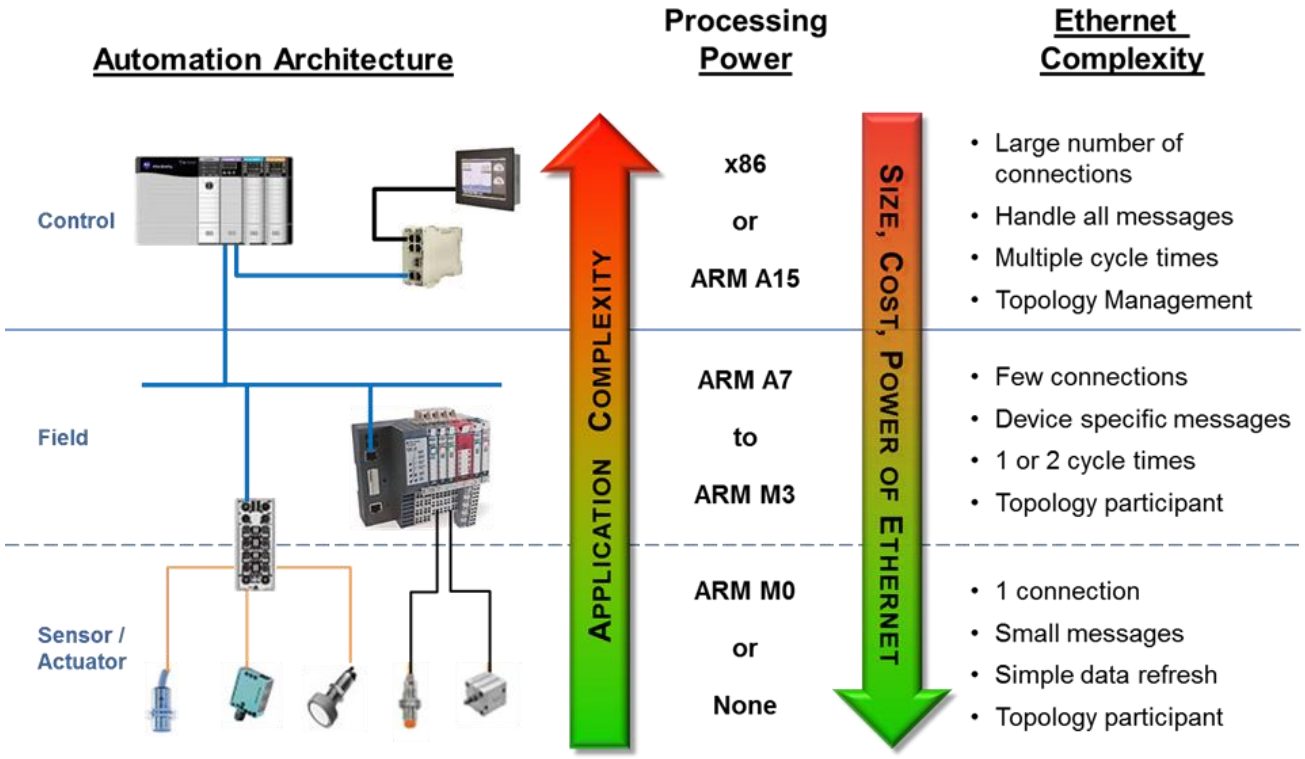
- Why isn't Ethernet at the Edge Today?
- Architecture of an Ethernet Node
- Scaling an Ethernet Node
- Example of a Low-complexity Ethernet Node
- Future Directions
- Conclusion

Ethernet in Automation



- Twisted Pair
- Distance (1km)
- Power
- Intrinsically Safe

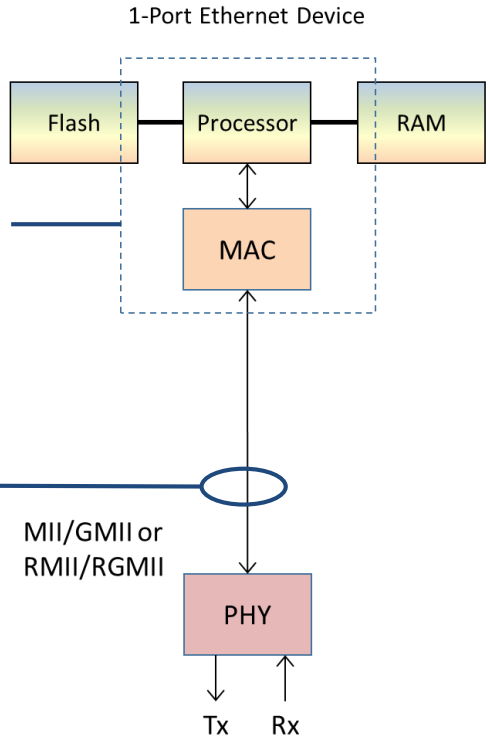
Automation Architecture vs. Ethernet Complexity

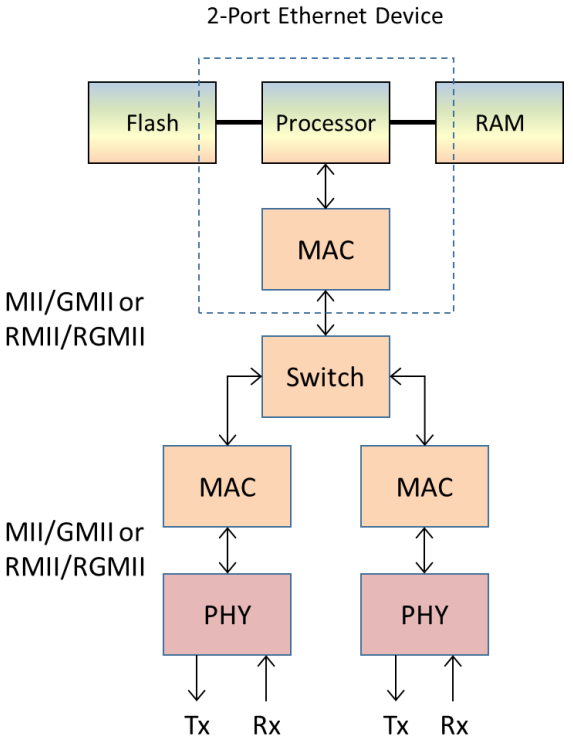


Architecture of an Ethernet Node

- MAC filter logic of limited use
- Process most Ethernet frames
- Protocols increase Flash / RAM

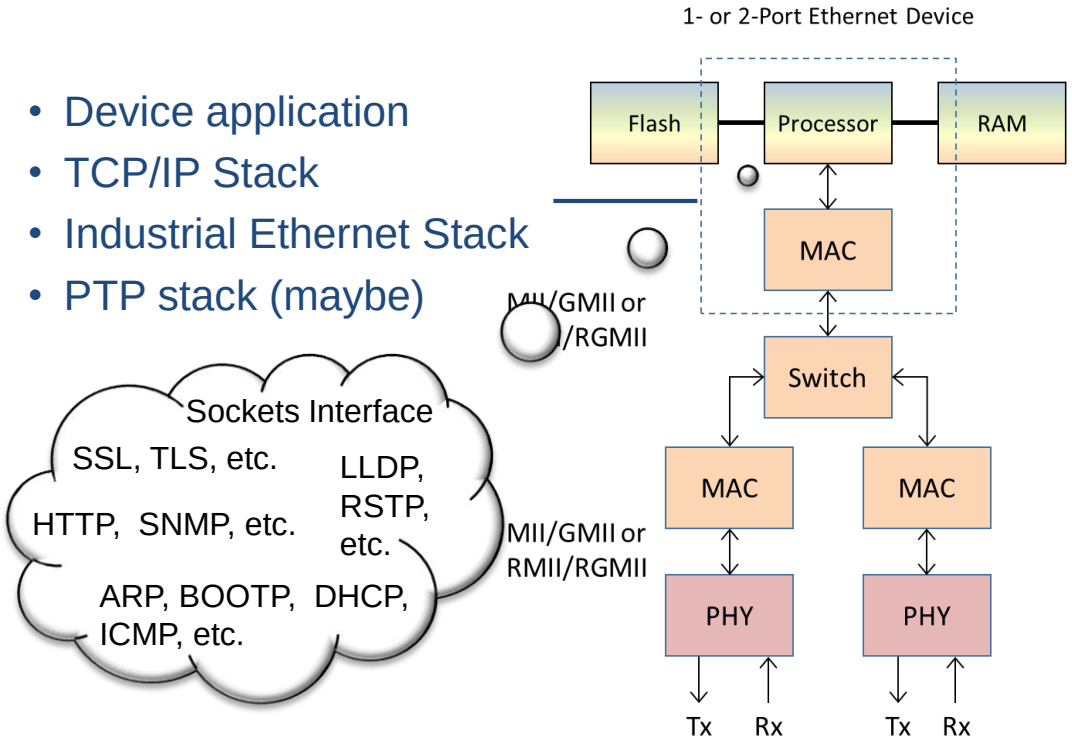
- Numerous high-speed pins
- Special layout considerations
- Hard to provide isolation





Mapping Ethernet to Node Architecture

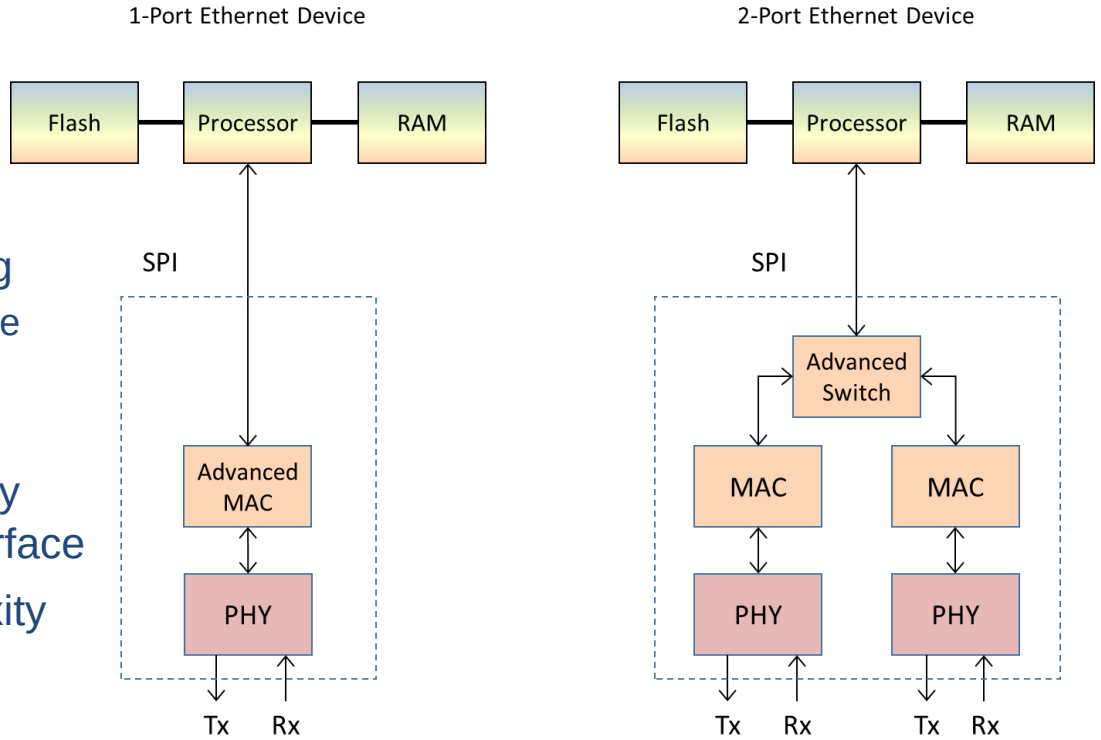
- Device application
- TCP/IP Stack
- Industrial Ethernet Stack
- PTP stack (maybe)



Layer	Type	OSI Model	TCP/IP Model	Authority
7	Data	Application Layer	Application Layer	RFCs, IETF, Industry Org's, etc.
6	Data	Presentation Layer		
5	Data	Session Layer		
4	Segments	Transport Layer	TCP / UDP	
3	Packets	Network Layer	IP	
2	Frames	Data Link Layer	Ethernet	IEEE 802.1
1	Bits	Physical Layer		IEEE 802.3

Scaling An Ethernet Node for Low-complexity

- Target small-scale single-chip processing solution by reducing
  - Processor speed / performance
  - Flash memory size
  - RAM size
- Reduce interconnect complexity from processor to network interface
- Reduce pin-count and complexity of network interface



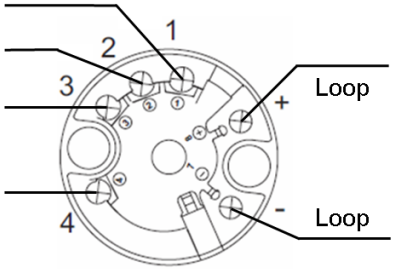
Advanced MAC / Switch

- Instead of general filtering…
  - ➢ perform intelligent / dynamic frame filtering and buffering before any frames are communicated to the processor
- Manage priorities among protocols
  - i.e. this ARP request isn't for me, don't send on
  - i.e. this ARP request in lower priority than incoming EtherNet/IP implicit message, send EtherNet/IP message first
- Manage surges in frame receipt due to alignment of various protocols
- ***Benefits***
  - Reduces overall buffer space
  - Retain frames based on priority, application state, and processor load conditions
  - Substantially reduces the amount of data transferred to and processed by the processor

Example Device with Low-complexity Ethernet

4..20 mA with HART

Connections for:
- 2-wire Potentiometer / RTD
- 3-wire Potentiometer / RTD
- 4-wire Potentiometer / RTD
- Voltage Measurement
- Thermocouple



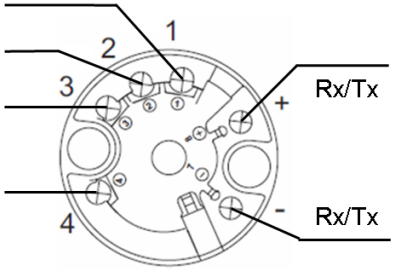
4..20 mA
- ➢ Process Variable (Temperature)

HART
- ➢ Calibration
- ➢ Alarms
- ➢ Set Points

Supply Power: 12..42V
Power Consumption: < 1.5W
Cable length: up to 3km
Bandwidth: 1200 Baud

Ethernet with future 2-wire

Connections for:
- 2-wire Potentiometer / RTD
- 3-wire Potentiometer / RTD
- 4-wire Potentiometer / RTD
- Voltage Measurement
- Thermocouple



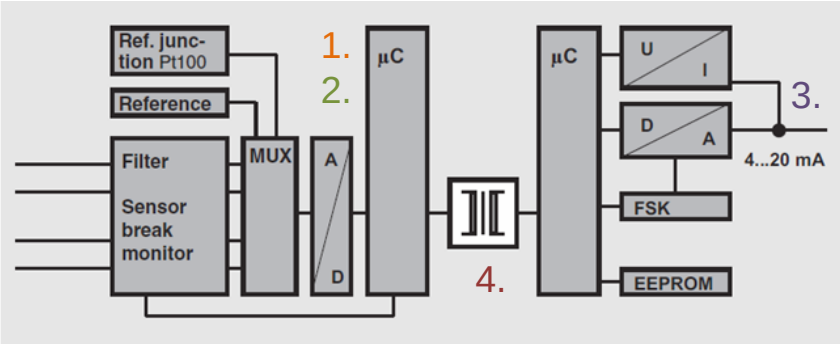
Ethernet
- ➢ Process Variable (Temperature)

Ethernet
- ➢ Calibration
- ➢ Alarms
- ➢ Set Points

Supply Power: 12..42V
Power Consumption: < 1.5W
Cable length: 200m..1km
Bandwidth: 100Mb/s..10Mb/s

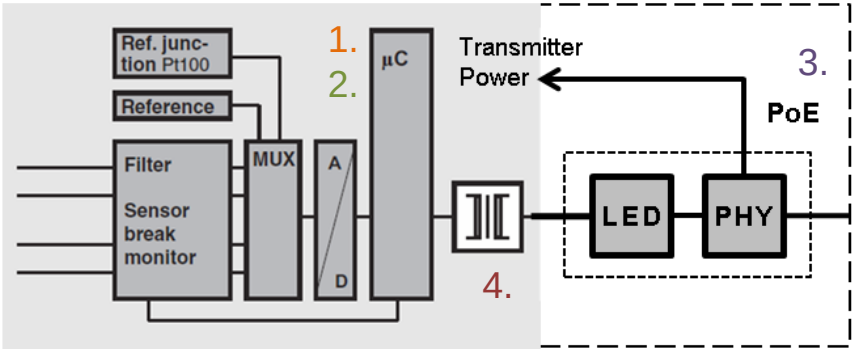
Example Device Architecture

Architecture using current 4..20mA



(Source: ABB, "Industrial Temperature Measurement Basics and Practice")

Architecture using Low-complexity Ethernet concept



Low-complexity Ethernet concept provides similar:

1. Processing power
2. Memory footprint
3. Total power budget
4. Simple isolation scheme

Future Directions

- Reducing the footprint of Ethernet opens the door to other possibilities
- PHY-related
  - Ethernet over twisted-pair
  - Adding power
  - Adding Intrinsic safety
  - ➢ Will the IEEE 10SPE effort get us these?
- Processor-related
  - Nano-stacks
  - IP-to-the-Edge versus Ethernet-to-the-Edge
    - i.e. stack versus no stack
- TSN down to the edge

Summary

- The goal of low-complexity Ethernet is to reduce the power, area, and cost of Ethernet
  - It is a concept to bring Ethernet to resource constrained devices that may not even have a MAC
- Device software has the biggest impact on complexity
  - Software footprint directly affects memory size – both Flash and RAM
  - The number and type of protocols directly affects processor selection
- Device hardware can be architected to help software manage complexity
  - Advanced MACs can offload software by providing more layer 2 processing
  - MAC / Processor Interface can be simplified from traditional MII
- Reallocating the MAC layer from the processor into the PHY creates the opportunity for the simplest processors to connect to Ethernet networks
- By using techniques previously identified (by Xu and Brooks), EtherNet/IP can be scaled and placed on top of the concept of low-complexity Ethernet

THANK YOU