

New Development on CompoNet Implementation

Toshiyuki Kojima
Omron Corporation

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Abstract:

This paper presents new technical developments and approaches on further reducing cost, size and implementation effort for CompoNet units. The cost reduction and downsizing need improvement on communications components. This time we have examined three possibilities: downsizing pulse transformers, using 3.3-V transceivers, incorporate CPU function in ASIC. With these improvements, CompoNet units become much compact, and can be implemented more cost-effectively with fewer implementation efforts.

Keywords:

CompoNet, Physical layer, Transceiver, Pulse transformers, ASIC

1 Introduction

CompoNet was designed as a CIP field network for applications dominated by sensors and actuators. The network exhibits all functions required for the communications of sensors and actuators level: easy installation, bit level data processing, connection with multiple nodes, high speed communications, and messaging. Especially in messaging, it uses the same protocol, CIP, as other ODVA family networks, such as EtherNet/IP and DeviceNet.

As for a sensor and actuator network, CompoNet vendors may need to customize their device implementation to pursuing further cost reduction, size reduction and implementation flexibility.

This paper presents new technical developments and approaches on further reducing cost, size and implementation effort for CompoNet units. The cost reduction and downsizing need improvement on communications components. This time we have examined three possibilities: downsizing pulse transformers, using 3.3-V transceivers, incorporate CPU function in ASIC. With these improvements, CompoNet units become much compact, and can be implemented more cost-effectively with fewer implementation efforts to meet vendor's requirements.

2 Currently Available CompoNet Chip Sets

2.1 Physical layer components

The main components of physical layer part of CompoNet include pulse transformers and RS485 transceivers. The type of pulse transformers to be used is specified in the ODVA CompoNet Specifications. Currently available transformers are not small enough to satisfy all applications. Also, currently available transceivers use 5-V power supply voltage, but some vendors may prefer to 3.3V power supply in their products.

The examination was made on how to use a much smaller pulse transformer and a 3.3V RS485 transceiver for CompoNet.

2.2 ASIC and CPU

CompoNet needs an ASIC for fast communications process, and a CPU for complicated message process. Currently available chip sets consist of CPU and ASIC separately.

The examination was made on how to integrate those two, ASIC and CPU, into a single chip and what should be considered.

3 Examination of Physical Layer Components

3.1 Criteria for physical layer components

The physical layer components to be chosen must satisfy these four requirements defined in the *CIP Network Library, Volume 6 (Rev 1.3)*.

1) Transmission mask

As one of the slave specifications, the criterion for amplitude that influences the physical layer performance is shown in the Table 1.

Table 1 Amplitude

	(Voltage)
Amplitude after waveform is stabilized	1.57 – 2.12

2) Transmission impedance

Table 2 specified the slave specifications.

Table 2 Slave Impedance during Transmit

Frequency	Impedance (Ohms)
750 kHz	137 - 160
1 MHz	143 - 166
1.5 MHz	154 - 180
3 MHz	181 - 210
4 MHz	194 – 225

3) Receive mask

Figure 1 illustrates one of the multiple specifications for the receive mask. The vertical axis in the following figures is ($V_{BDH} - V_{BDL}$). From the figure, it can be stated the transceiver must have the sensitivity of ± 60 mV in reception performance. CompoNet Specifications includes some margins and defines it as ± 50 mV.

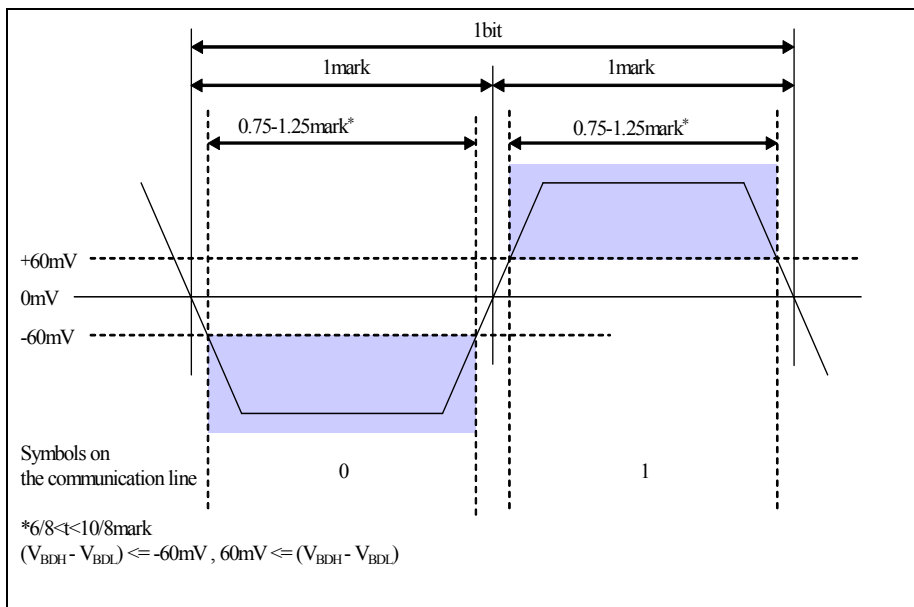


Figure 1 Receive Mask

- 4) Receive impedance
Table 3 specified the slave specifications.

Table 3 Slave Impedance during Receive

Frequency	Impedance (Ohms)
750 kHz	847 - 985
1 MHz	821 - 955
1.5 MHz	754 - 877
3 MHz	558 - 649
4 MHz	477 - 554

3.2 RS485 transceiver of 3.3 V

3.2.1 Issues concerning 3.3V transceivers

The most important factor for a transceiver to satisfy the Receive mask is receiver sensitivity. Normally, a RS485 transceiver has receiver sensitivity in ± 200 mV. As CompoNet must receive attenuated waveforms, much higher sensitivity is required for the transceiver, i.e., ± 50 mV. To satisfy the sensitivity, the vender must be keen on selecting appropriate components and changing the design. Only a limited number of venders have such capacity. The other factor to be examined is if both amplitude and transmission impedance can be satisfied at the same time. To get the same amplitude for 3.3V power voltage as for 5V, the output resistance element must be reduced so that the voltage drop is minimized. This, however, declines the transmission impedance. Examination must be made on transceiver characteristics and circuit constant, and to see if the both criteria can be satisfied simultaneously. The inductance of transformer is considered to decrease when the pulse transformer is downsized. Decline of inductance gradually lowers the waveforms. It must be examined that the compact transformer can satisfy the transmission mask.

3.2.2 Selecting RS485 transceivers of 3.3V

In order to satisfy the criterion of transmission impedance, the transceiver must not generate current when the output is low. An IC should be selected to satisfy the above characteristic and higher receiver sensitivity. VI curves of 3.3-V transceivers for the IC are shown in below. The IC may be modified by the manufacturer to have high impedance and not to generate current when the transceiver output is low.

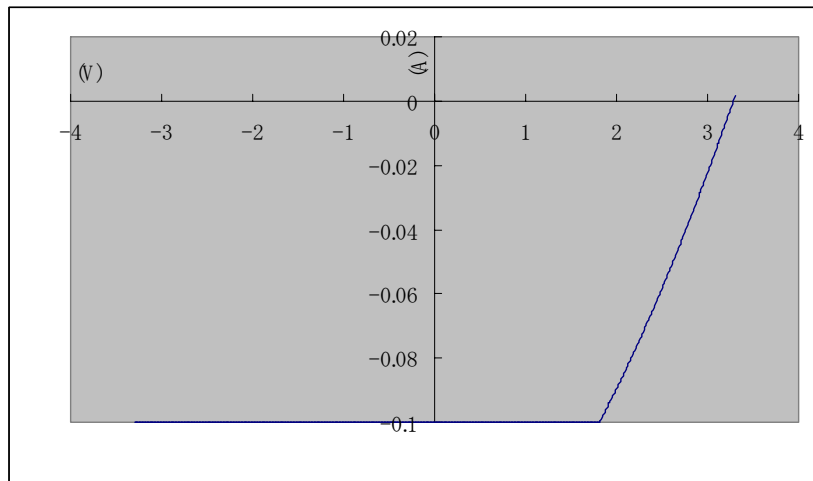


Figure 2 Output Current vs. Differential Driver Output Low Voltage

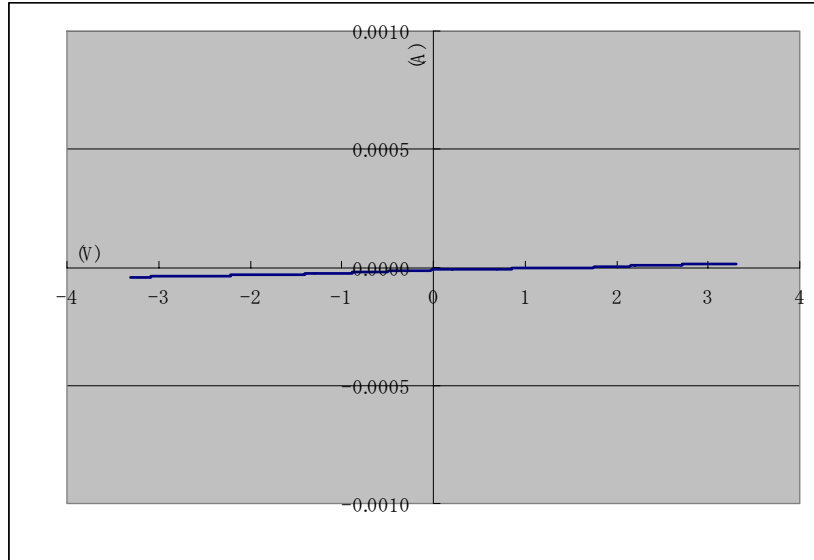


Figure 3 Output Current vs. Differential Driver Output High Voltage

As shown in Figure 2 and 3, creation of IBIS (I/O buffer information specification) models and having precise simulations became possible. Figure 2 can tell the transceiver characteristic is nearly straight when the output is high. Thus the transceiver output can be approximated as shown in Figure 4.

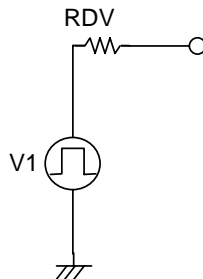


Figure 4 Approximated circuit for transceiver

From Figure4, $RDV = 14 \Omega$.

3.2.3 Examination by theoretical formula

The Figure 5 illustrates the basic circuit of CompoNet in transmission.

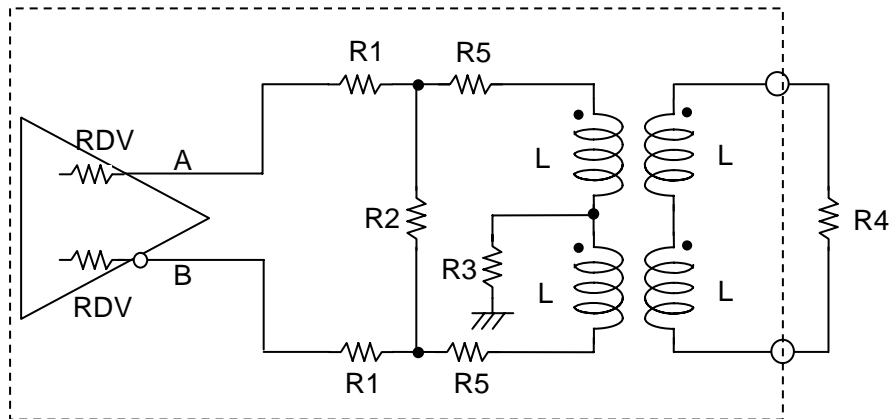


Figure 5 Basic circuit of CompoNet

Coils and capacitors are added to reduce noise. The circuit in Figure 5 was used for the examination. Current must not be generated when the transceiver output is low. Thus the terminals outputting low have high impedance. The transmission circuit connected with an 85 Ω load is shown in Figure 6.

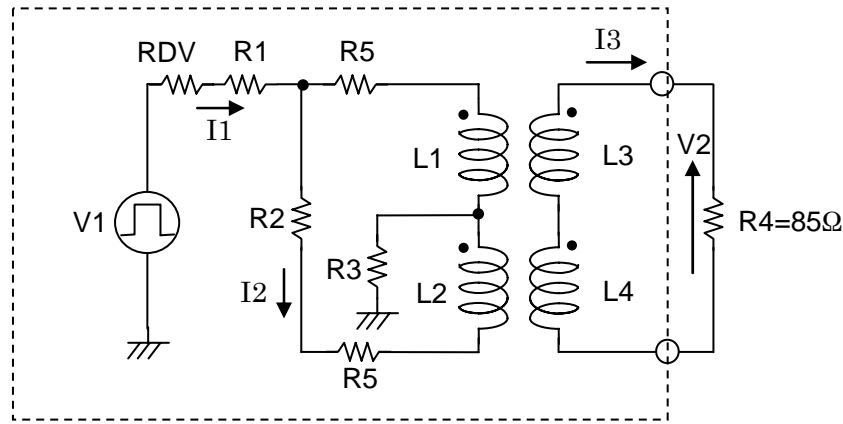


Figure 6 Circuit at transmission

The calculation formula with Laplace transformation is as follows:

$$\begin{pmatrix} sL + RDV + R1 + R3 + R5 & -s(1+k)L - R5 & -2skL \\ -s(1+k)L - R5 & 2s(1+k)L + R2 + 2R5 & 4skL \\ -2skL & 4skL & 2s(1+k)L + R4 \end{pmatrix} \times \begin{pmatrix} I1 \\ I2 \\ I3 \end{pmatrix} = \begin{pmatrix} V1 \\ 0 \\ 0 \end{pmatrix}$$

Where k is the combination coefficient.

The current $I3$ is given by the above formula and inverse matrix. The determinant of matrix is expressed by Delta, Δ .

$$I3 = \frac{2kL \times R2}{\frac{1}{s} \cdot \Delta} \times V1$$

$$\frac{1}{s} \cdot \Delta = as^2 + bs + c + ds^{-1}$$

When the frequency domain is considered:

Regarding the term $(as^2 + bs)$, the greater the frequency is, the greater the Delta and the lesser the $I3$ are. That is the low pass filter of the secondary side. Regarding the ds^{-1} , the lesser the frequency is, the greater the Delta and the lesser the $I3$ are. That is the high pass filter of primary side. Therefore, we only have to consider the term c for the flat part of midrange frequency. The term c is obtained by the following formula:

$$c = R4 \cdot (R2 + 2R5) + 2 \cdot (1+k) \cdot (RDV + R1 + R3) \cdot (R2 + R4 + 2R5) + 2 \cdot (1+k) \cdot R5 \cdot (R2 + R5)$$

As k is almost 1, it is regarded as 1.

$$V2 = R4 \cdot I3 = \frac{2 \cdot R2 \cdot R4}{R4 \cdot (R2 + 2R5) + 4 \cdot (RDV + R1 + R3) \cdot (R2 + R4 + 2R5) + 4 \cdot R5 \cdot (R2 + R5)} \times V1$$

The next step is to calculate the transmission impedance (R_{out}) and the Receive impedance (R_{in}) for physical layer. The Thevenin's theorem is applied for the above formulas used to have $V2$ and $I3$. R_{out} can be obtained by $V2$ when the $R4$ is infinite and by $I3$ when $R4$ is 0.

$$R_{out} = \frac{V2(R4 = \infty)}{I3(R4 = 0)} = \frac{4 \cdot (RDV + R1 + R3) \cdot (R2 + 2R5) + 4 \cdot (R2 + R5) \cdot R5}{(R2 + 2R5) + 4 \cdot (RDV + R1 + R3)}$$

Rin is the case when both terminals of A and B on the transceiver have high impedance. Thus it is the value when R1 is infinite.

$$R_{in} = \frac{2 \cdot R_2}{(R_2 + 2 \cdot R_5) + 4 \cdot (RDV + R_1 + R_3)}$$

The CompoNet Specification has already determined the value V2, Rin and Rout.

When the case supposes 1.5 MHz, they are:

RDV=14 Ω, R4=85 Ω, V1=3.3 V, V2=1.845 V, Rin=815.5 Ω, Rout=167 Ω.

Using the above formula, the resistance constants in the salve units, (R1+R3), R2 and R5 are calculated:

$$R_2 = \frac{2 \cdot R_4 \cdot V_1 \cdot (R_{in} - R_{out})}{V_2 \cdot (R_4 + R_{out})} = 782$$

$$R_1 + R_3 = \frac{R_2 \cdot R_4 \cdot V_1}{2 \cdot (R_4 + R_{out}) \cdot V_2} - \frac{R_{in}}{4} - RDV = 18$$

$$R_5 = \frac{R_{in} - R_2}{2} = 16.75$$

The above is the case in 1.5 MHz. The CompoNet Specifications supposes the transmission impedance and the Receive impedance in 750 kHz, 3 MHz and 4 MHz. If no capacitor and coil are used, impedance is independent from frequency. Therefore, it is estimated the case using other frequency than 1.5 MHz can satisfy the requirement by adjusting capacitor and coil that are adopted for noise reduction.

As long as the satisfactory resistance is obtained, the RS485 transceiver of 3.3 V can also meet the criteria of selecting components. Thus it can be used for CompoNet.

The theoretical formulas were confirmed by circuit simulation. In simulation, R1 = 18 Ω, R2 = 782 Ω, R3 = 0 Ω, R5 = 16.75 Ω, RDV = 14 Ω, L1 = L2 = L3 = L4 = 3.75mH, the combination coefficient for transformers, k, is 1, V1 = 3.3 V and the frequency is 1.5 MHz. The simulation result is shown in Table 4.

Table 4 Simulation result

Theoretical calculation			Simulation result		
Amplitude	Transmission impedance	Receive impedance	Amplitude	Transmission impedance	Receive impedance
1.845	167	815.5	1.841	167.4	809.3

The result almost conforms to the theoretical calculation, and attests it is correct.

3.3 Examination of downsizing pulse transformers

3.3.1 Issues concerning pulse transformers

The issue that hinders downsizing the pulse transformers is that it lowers the inductance due to having a less number of wire turns and a smaller cross section. Lower inductance gradually deteriorates the waveforms. It may hamper the expected output amplitude in baud rate of 93.75 kHz. The other parameters in the transformers are irrelevant to its size and profile. The inductance is the only factor we have to consider. The present CompoNet Specification defines 1.625 mH as the inductance on a transformer with one wire turn. If the lower inductances can satisfy the CompoNet specifications, it means downsizing the transformer is acceptable.

3.3.2 Criteria for pulse transformers

The CompoNet Specifications defines the amplitude ranges 1.57 and 2.12 V while R4 = 85 Ω. The pulse duration in baud rate of 93.75 KHz is 5.4μs. Thus the voltage drop at L during 5.4μs is made lower than 0.275 V, which is half of the amplitude. It means a transformer is selected to have a lower ratio of voltage drop due to inductance than 0.275/1.845=15%.

3.3.3 Examination by theoretical formula

A slave circuit was used to examine the waveform deterioration due to inductance at transmission. In Figure 5, R2 value is too great to ignore the influence by L2. The equivalent circuit seen from primary side appears as in below:

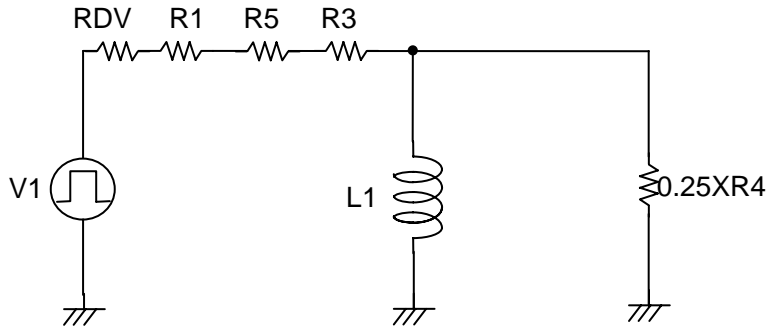


Figure 7 Equivalent circuit seen from primary side of transmission

The deterioration ratio, D , after t_1 time passes is calculated by the formula:

$$D = 1 - e^{-\frac{0.25 \cdot RA \cdot R4}{(RA + 0.25 \cdot R4) \cdot L1} t_1}$$

where $RA = RDV + R1 + R5 + R3$.

When $RDV = 14 \Omega$, $R1 = 18 \Omega$, $R5 = 16.75 \Omega$, $R3 = 0$, $R4 = 85 \Omega$ and $t_1 = 5.4 \mu s$, $L1$ must be greater than $0.49 mH$ to satisfy the deterioration ratio of 15%.

The present transformer has $1.625 mH$ minimum. It demonstrates decreasing the inductance, i.e., downsizing the pulse transformer, is acceptable.

3.4 Confirmation by simulation

The above theoretical calculation is to examine the parameter which gives a large influence to the characteristic. There are other parameters of components for noise reduction. A simulation was conducted to see overall conformity. The specified values in transmission impedance and Receive impedance differ by frequencies. The capacitor and coil are tuned to align with the specified values. Figure 8 shows the CompoNet circuit.

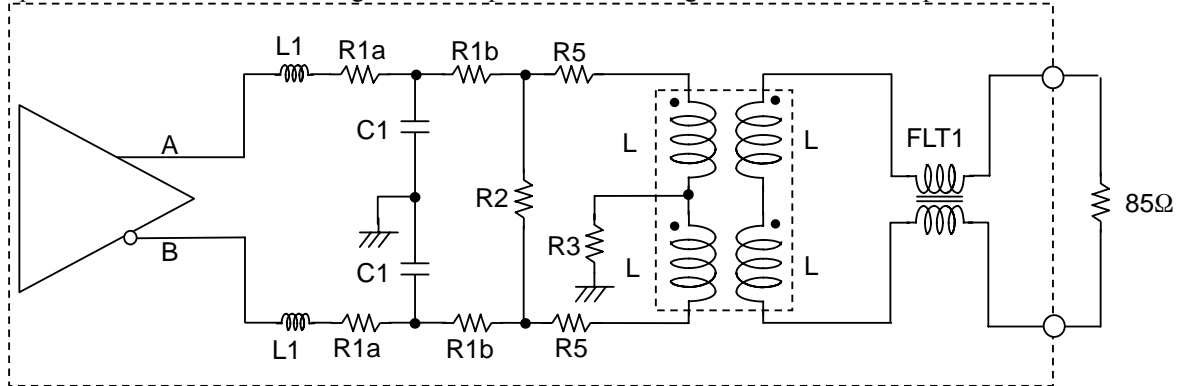


Figure 8 CompoNet circuit

The FLT1 is used for noise reduction. Based on the data obtained by Figure 2 and 3, IBIS models were created for 3.3-V transceivers. The vendor provided a FLT1 model. The examination result in 3.3 tells the transformer inductance must be greater than $0.49 mH$. To have some margin, we set it in $0.8 mH$. Other parameters were set as follows: $k = 0.9995$, the coil resistance is 1.5Ω , and the capacitance between primary and secondary coils is $30 pF$. The Receive impedance is influenced by $C1$ but not by $L1$. Thus the frequency influence is adjusted by $C1$. The transmission impedance is influenced both by $C1$ and $L1$. Therefore after $C1$ is determined by the Receive impedance, the frequency influence on the transmission impedance is adjusted by $L1$. The resistance $R1$ and $R2$ must also be modified.

The following section reports the result of simulation on slaves. Table 5 shows the result where $R1a = R1b = 5.1$, $R2 = 910$, $R3 = 0$, $R5 = 16$, $C1 = 130$ pF, and $L1 = 1$ μ H. The results of amplitude, Receive impedance, and transmission impedance are acceptable in all frequencies.

Table 5 Simulation result

Frequency (Hz)	CompoNet specification			Simulation result		
	Amplitude	Transmission impedance	Receive impedance	Amplitude	Transmission impedance	Receive impedance
750K	1.57-2.12	847-985	137-160	2.059	920.69	155.7
1M		821-955	143-166		890.97	157.2
1.5M		754-877	154-180		818.32	161.5
3M		558-649	181-210		599.53	184.5
4M		477-554	194-225		490.47	208.7

Figure 9, Figure 10 and Figure 11 show the simulation waveforms.

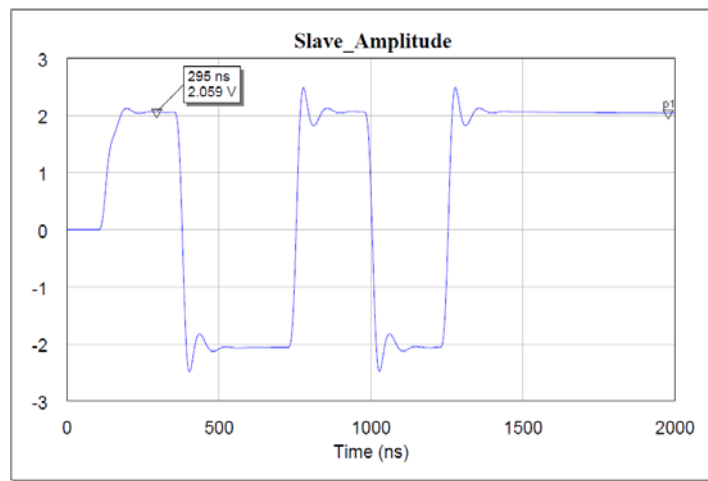


Figure 9 Simulation result (amplitude waveform)

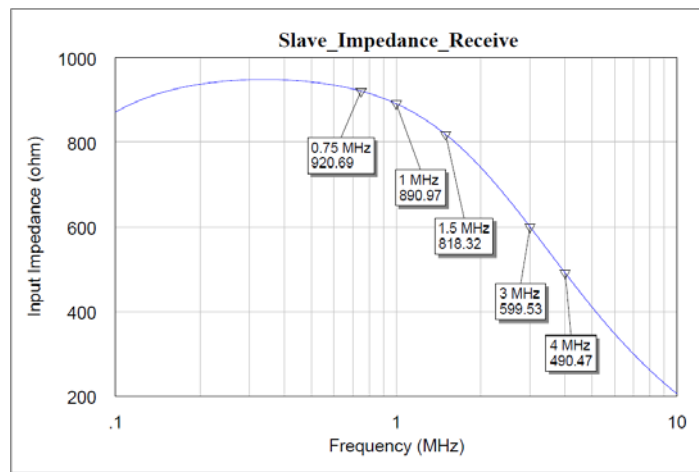


Figure 10 Simulation result (Impedance at Receive)

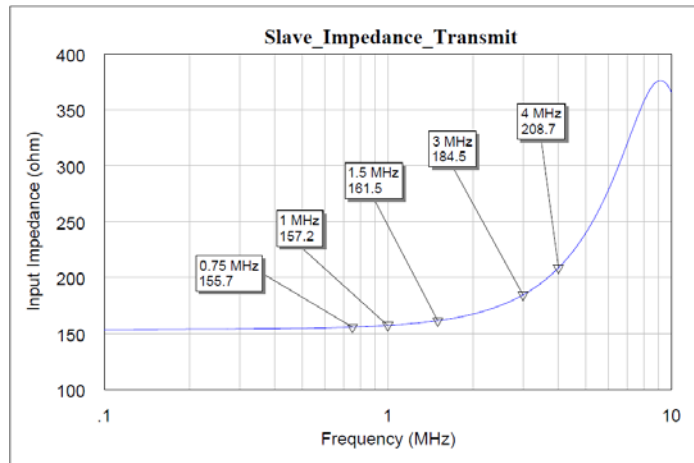


Figure 11 Simulation result (Impedance at transmission)

4 Examination of an ASIC incorporating CPU function

4.1 Issues and solution concerning ASIC

The present CompoNet implementation must have two elements: one is ASIC for processing high speed communications, and the other is CPU for processing CIP.

Can we realize CompoNet in a single chip? Examination was made on how to incorporate CPU function internally into the ASIC, for example, of bit level digital I/O slave units.

4.2 Requisite functions for an bit-slave ASIC incorporating CPU function

The functions required for an bit-slave ASIC incorporating CPU functions include:

- Data processing of 4-point IN/OUT
- Object implementation requirements for CompoNet discrete I/O
- MS/NS indicators, and switch setting of MAC IDs
- EEPROM access
- Watchdog timer to detect CPU overrun

To maintain the low cost objective, the gate size and the capacity of ROM and RAM must be minimized as small as possible.

4.3 Example of ASIC incorporating CPU function

This section exemplifies an ASIC that incorporates the CPU functions and mounts the above mentioned requisite functions as well. The IP core of Z80 compatible CPU, which operates in 16 MHz, was used, because the gate is extremely small. The internal block diagram is shown in Figure 12.

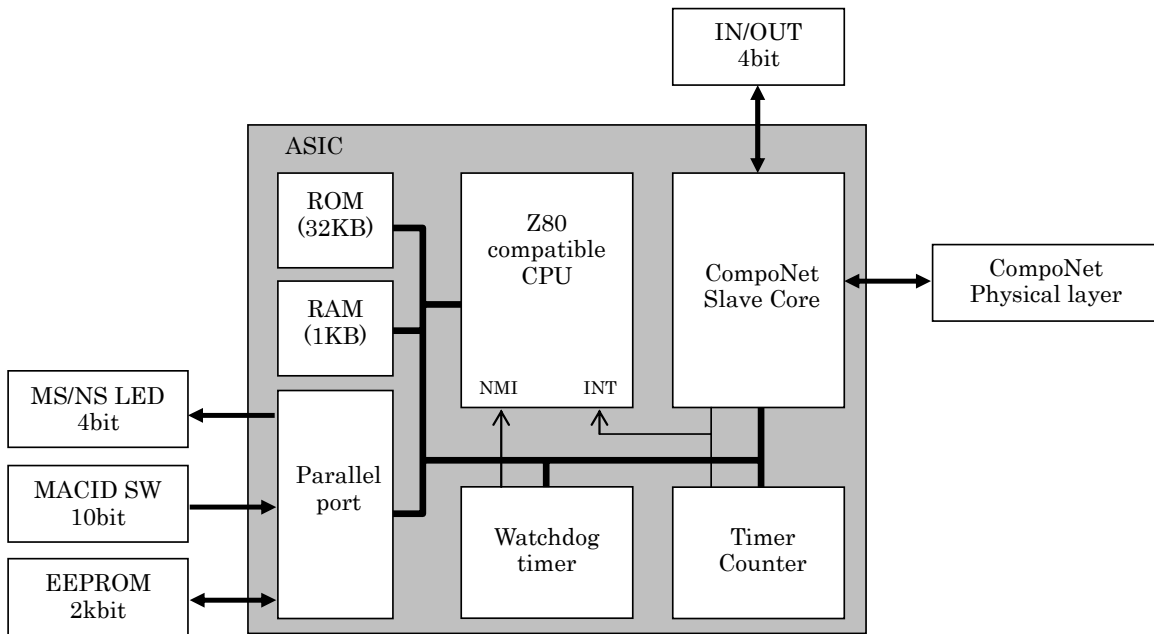


Figure 12 Example of ASIC incorporating CPU function

In this way software is feasible with the Z80 compatible CPU in 16 MHz, a 32-KB ROM, and a 1-KB RAM. This proves that an extremely small ASIC can incorporate CPU functions, and that the further device cost reduction and downsizing is achievable.

5 Conclusion

The examinations described in this paper presented the way for how to design your own components in CompoNet physical layer, ASIC and CPU and for improving the chip sets. As for the issues concerning the physical layer, simulation was only made for the element alone. Verifications shall be made with actual components and by connecting in a system.

References:

ODVA, Inc., Volume 6 CompoNet Adaptation of CIP

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