



Developer's Introduction to CompoNet:

Design Considerations for CompoNet
Processors

Tools Track

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Introduction

This section aims to introduce how to choose your own CPU for 2 types of OMRON's ASIC.

Disclaimer: The information here is just for reference. No guarantee of proper operation.

Agenda:

- ▶ The differences of the 2 types of ASIC
- ▶ Overview of TF542NG
- ▶ A TF542NG Analysis Example
- ▶ Overview of TF547NF
- ▶ A TF547NF Analysis Example

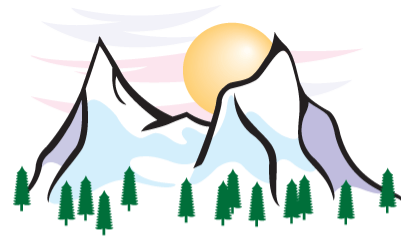
ASIC Type

2 types of slave ASIC available: TF542NG and TF557NF.

▶ Main Differences:

	Device Category	I/O capability	MPU-I/F	Package	Distributor
TF542NG	Slave/ repeater	256/ 256bits	16 bits	108BGA	OC, others
TF557NF	Slave	128/ 128bits	16/ 8bits	64TQFP	OC

- ▶ Driver firmware: compatible for slaves
- ▶ Tool kit: Samples of TF557NF are NOT included in the ODVA developer's toolkit



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MPU I/F in TF542NG ASIC for Slaves/Repeaters

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Overview of TF542NG

- ASIC for MPUs with 16-bit external address bus
- Applicable for slaves and repeaters

ASIC Interface Functions and Remarks

- Reads from/writes to registers and buffer area according to read/write control signal and address/data signals from MPU.
- support MPU with multiplex buses.
- Hardware wait output by RDY signal.
- Bus access, software wait, and hardware wait of MPU must be set in consistency with the ASIC requirements for bus access and AC timing.
- Full-decode of 16 address signals 0 to 15.
- Notifies frame transmission/reception on CompoNet network to MPU by outputting external interrupt using INT signal.

TF542NG Interface

Pins

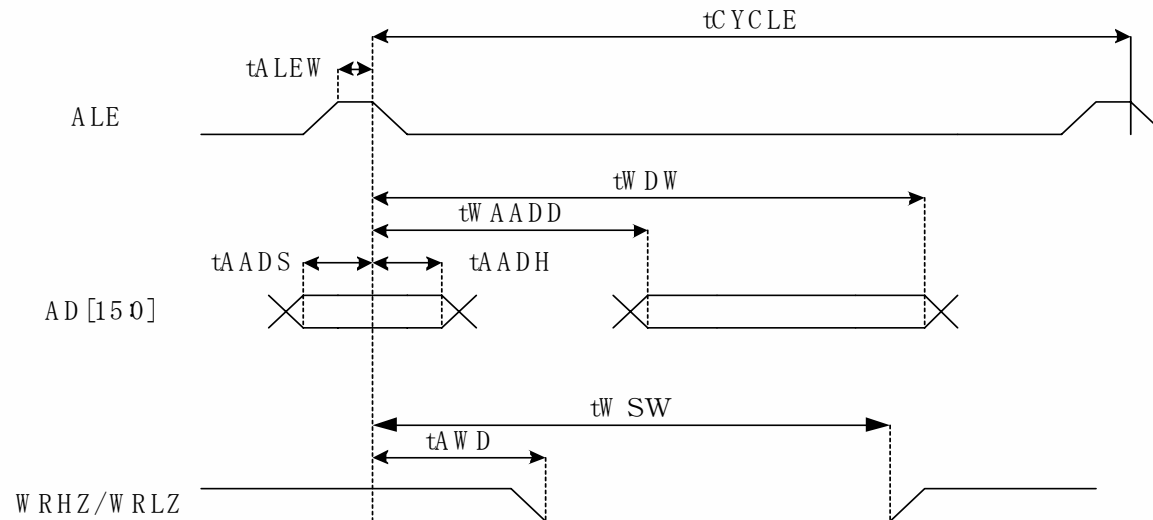
Pin Name	I/O	Description	True Value
WRHZ	IN	Write control of data bus upper 8 bits	L
WRLZ	IN	Write control of data bus lower 8 bits	L
RDZ	IN	Read control	L
ALE	IN	Address latch enable	H
AD15 to ADO	I/O	Address data bus	---
INT0Z	OUT	Interrupt	L
RDY	OUT	Hardware wait	L

Address Area

Byte Address	Area Name
2000h 20E3h	Registers
	Reserved (Data unspecified)
2100h 211Fh	INBuffer
2120h 213Fh	OUTBuffer
	Reserved (Data unspecified)
2160h 2191h	EventSendBuffer
	Reserved (Data unspecified)
21A0h 21D1h	EventReceiveBuffer
	Reserved (Data unspecified)

Attention: The ASIC address must be mapped to the area starting from xxx2000hex!

AC Timing of TF542NG: WRITE

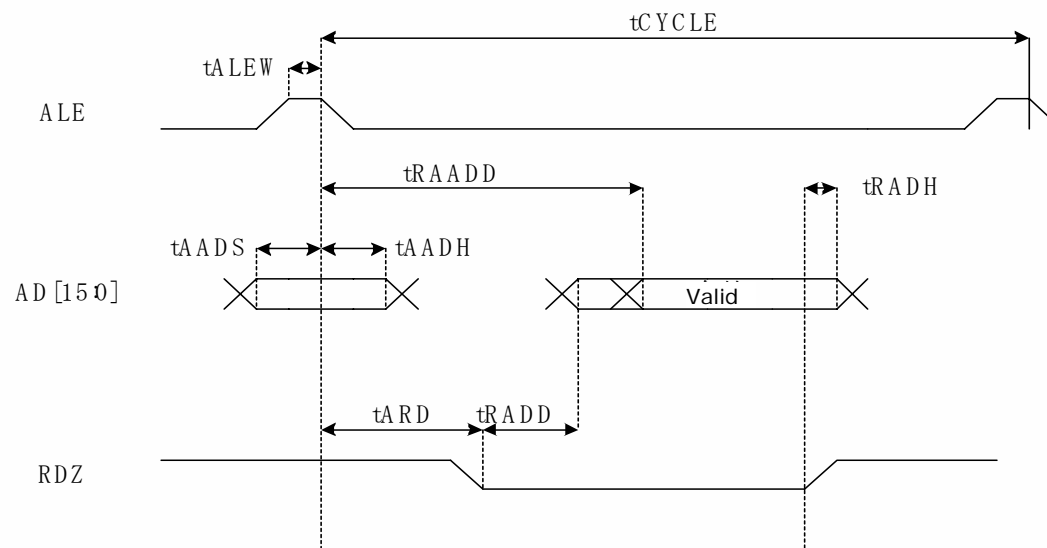


(VDD = 3.3 ±0.3V, TA = -40 to 85°C, CL = 15pF)

(unit: ns)

Item	Symbol	MIN.	MAX.
Cycle time	t_{CYCLE}	312	---
ALE width	t_{ALEW}	10	---
Address setup time	t_{AADS}	11	---
Address hold time	t_{AADH}	14	---
Write data delay time	t_{WAWD}	---	80
Write data valid time	t_{WDW}	170	---
Write signal delay time	t_{AWD}	---	80
Write signal valid time	t_{WSW}	170	---

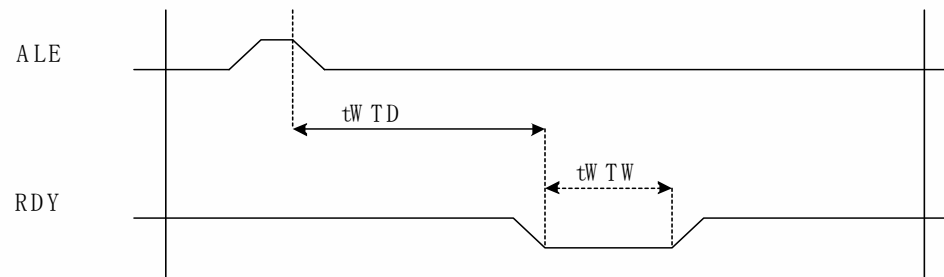
AC Timing of TF542NG: READ



(VDD = 3.3 ± 0.3V, TA = -40 to 85°C, CL = 15pF) (unit: ns)

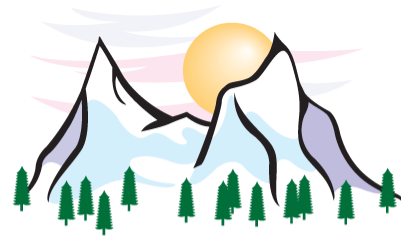
Item	Symbol	MIN.	MAX.
Cycle time	t_{CYCLE}	312	---
ALE width	t_{ALEW}	10	---
Address setup time	t_{AADS}	11	---
Address hold time	t_{AADH}	14	---
Read data disable time	t_{RADH}	8	---
Read signal delay time	t_{ARD}	---	50
Read data delay time (RD)	t_{RADD}	---	130

AC Timing of TF542NG: READY



(VDD = 3.3 ±0.3V, TA = -40 to 85°C, CL = 15pF) (unit: ns)

Item	Symbol	MIN.	MAX.
RDY signal delay	t_{WTD}	---	104
RDY signal width	t_{WTW}	---	134.8



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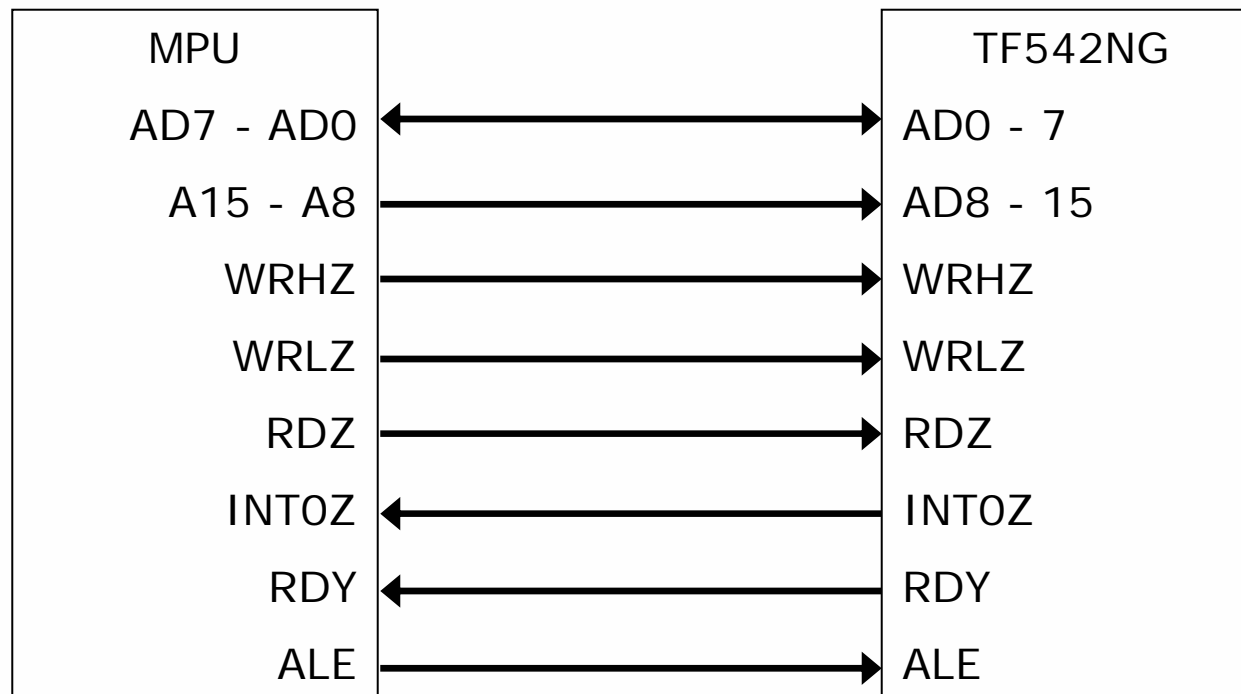
A TF542NG Analysis Example (no guarantee of proper operation)

**MPU manufactured by NEC
Model: uPD70F3716GC-8EA**

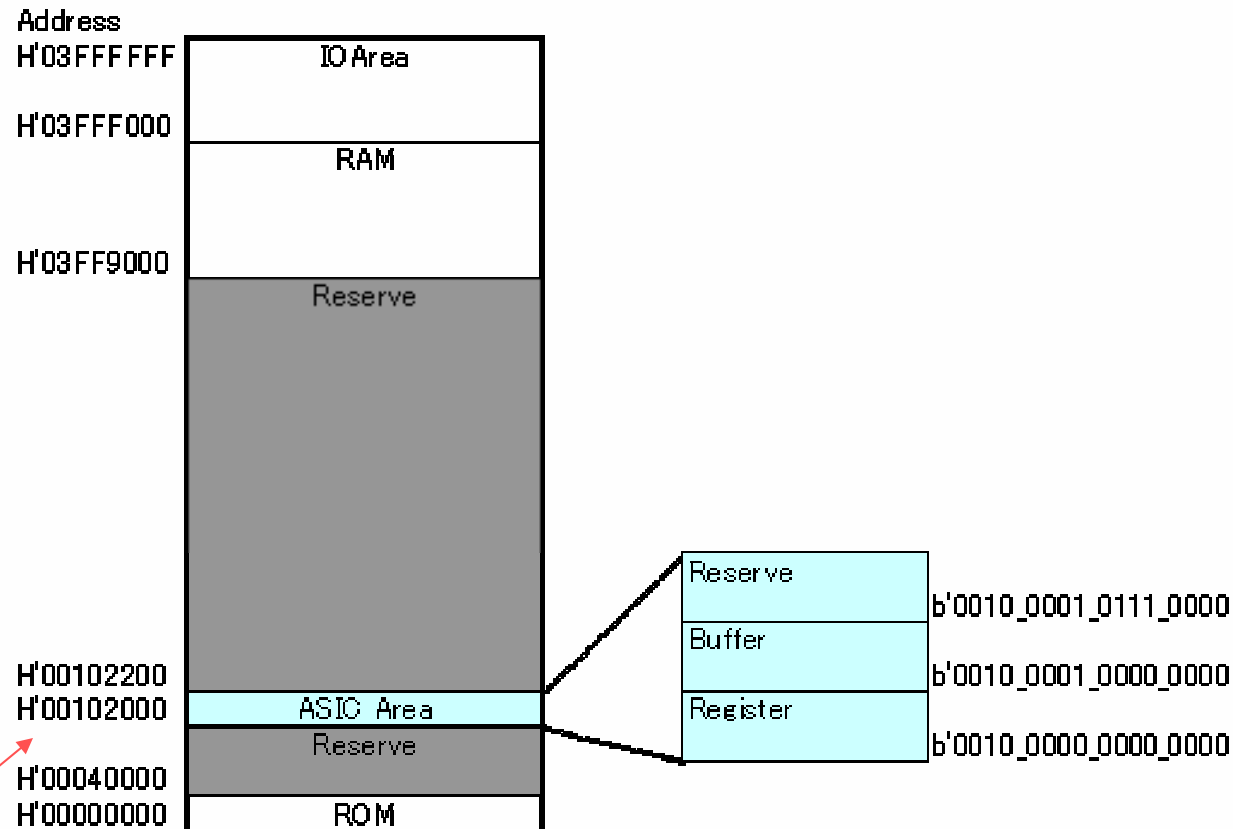
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Connection Image: uPD70F3716GC-8EA and TF542NG

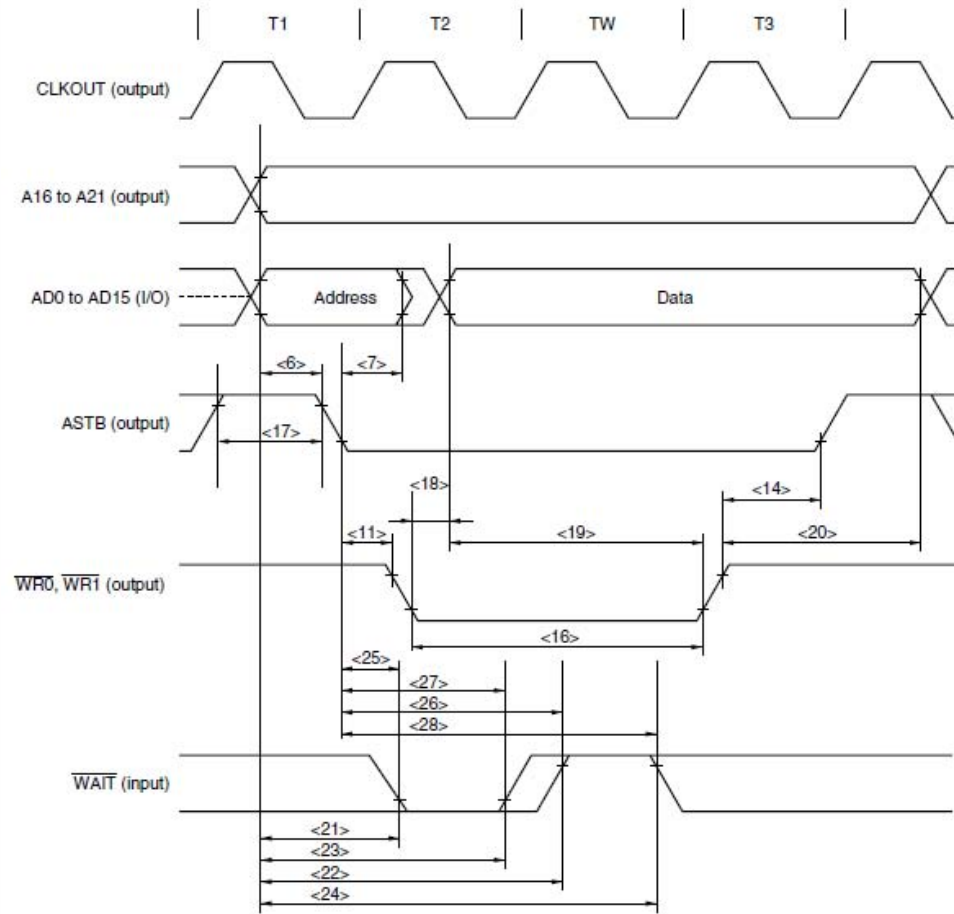


Memory Map: uPD70F3716GC-8EA



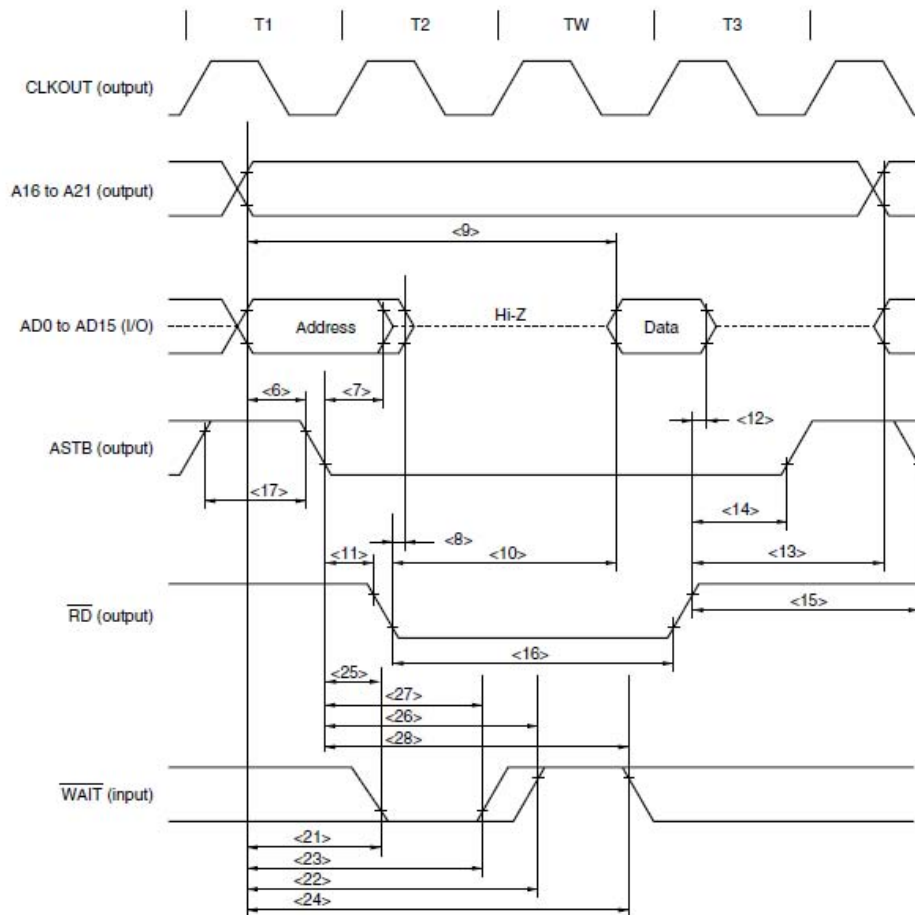
Attention: The ASIC address must be mapped to the area starting from xxx2000hex!

AC Timing of uPD70F3716GC-8EA: WRITE



Remark \overline{RD} is high level.

AC Timing of uPD70F3716GC-8EA: READ



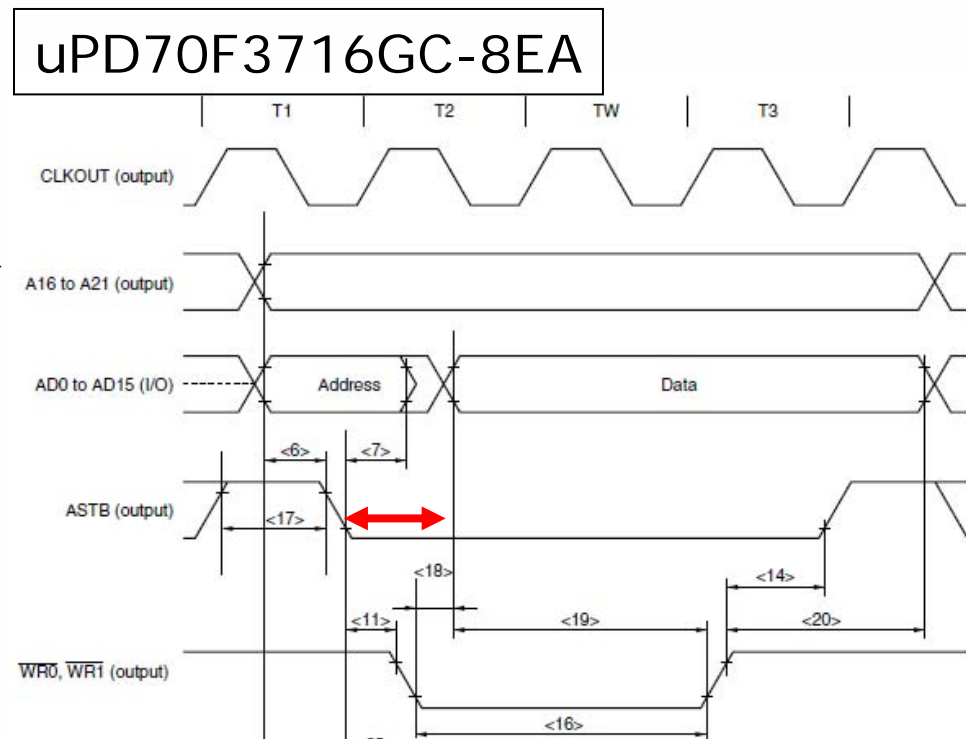
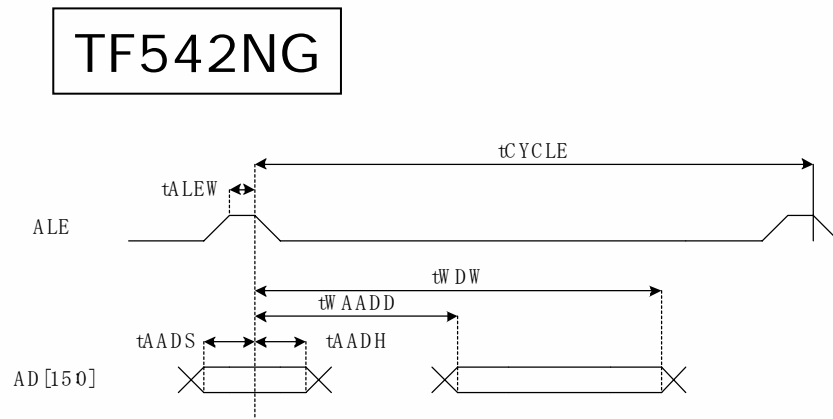
Remark $\overline{WR0}$ and $\overline{WR1}$ are high level.

AC Timing of uPD70F3716GC-8EA

(TA = -40 to +85°C, BVDD ≤ VDD = EVDD = AVREF0 = VREF1, VSS = EVSS = BVSS = AVSS = 0V, CL = 50pF) (unit: ns)

Item	Symbol/Mark		Condition	MIN.	MAX.
Address setup time (to ASTB ↓)	tSAST	6		$(0.5 + tASW)T - 20$	---
Address hold time (from ASTB ↓)	tHSTA	7		$(0.5 + tAHW)T - 15$	---
Delay time from RD ↓ to address float t	tFRDA	8			16
Data input setup time from address	tSAID	9			$(2 + n + tASW + tAHW)T - 35$
Data input setup time from RD ↓	tSRID	10			$(1 + n)T - 25$
Delay time from ASTB ↓ to RD, WRm ↓	tDSTRDWR	11		$(0.5 + tAHW)T - 15$	---
Data input hold time (from RD ↑)	tHRDID	12		0	---
Address output time from RD ↑	tDRDA	13		$(1 + i)T - 15$	
Delay time from RD, WRm ↑ to ASTB ↑	tDRDWRST	14		$0.5T - 15$	
Delay time from RD ↑ to ASTB ↓	tDRDST	15		$(1.5 + i + tASW)T - 15$	
RD, WRm low-level width	tWRDWRL	16		$(1 + n)T - 15$	
ASTB high-level width	tWSTH	17		$(1 + i + tASW)T - 15$	
Data output time from WRm ↓	tDWROD	18			15
Data output setup time (to WRm ↑)	tSODWR	19		$(1 + n)T - 20$	
Data output hold time (from WRm ↑)	tHWROD	20		$T - 15$	
WAIT setup time (to address)	tSAWT1	21	n ≥ 1		$(1.5 + tASW + tAHW)T - 35$
	tSAWT2	22			$(1.5 + n + tASW + tAHW)T - 35$
WAIT hold time (from address)	tHAWT1	23	n ≥ 1	$(0.5 + n + tASW + tAHW)T$	
	tHAWT2	24		$(1.5 + n + tASW + tAHW)T$	
WAIT setup time (to ASTB ↓)	tSSTWT1	25	n ≥ 1		$(1 + tAHW)T - 25$
	tSSTWT2	26			$(1 + n + tAHW)T - 25$
WAIT hold time (from ASTB ↓)	tHSTWT1	27	n ≥ 1	$(n + tAHW)T$	
	tHSTWT2	28		$(1 + n + tAHW)T$	

Example of Timing Verification uPD70F3716GC-8EA and TF542NG



Verification to conform Write Data Delay Time (t_{WAADD}) is less than 80
Corresponding time in NEC MPU is indicated by an red arrow.

$$\begin{aligned} &\langle 11 \rangle + \langle 18 \rangle \\ &= t_{DSTRDWR} + t_{DWROD} \\ &= \langle t_{CYK} * (1/2 + t_{AHW}) - 15 \rangle + \langle 15 \rangle \\ &= 31.25 < 80 \end{aligned}$$



OK!



Timing Verification Results

uPD70F3716GC-8EA and TF542NG

WRITE

ASIC Requirements				Verification for NEC MPU			
Item	Symbol	MIN.	MAX.	Corresponding Time	Calculation	Result	Evaluation
Cycle time	tCYCLE	312		---	$TCYK * (3 + tASW + tAHW + n + i)$	375	OK
ALE width	tALEW	10		tWSTH	$TCYK * (1 + i + tASW) - 15$	110	OK
Address setup time	tAADS	11		tSAST	$TCYK * (1/2 + tASW) - 20$	73.75	OK
Address hold time	tAADH	14		tHSTA	$TCYK * (1/2 + tAHW) - 15$	16.25	OK
Write data delay time	tWAADD	---	80	tDSTRDWR + tDWROD	$TCYK * (1/2 + tAHW) - 15$	31.25	OK
Write data valid time	tWDW	170		tDSTRDWR + tWRDWR + tHWROD	$TCYK * (1/2 + tAHW) - 15 + TCYK * (1 + n) - 15 + TCYK * 1 - 15$	236.25	OK
Write signal delay time	tAWD		80	tDSTRDWR	$TCYK * (1/2 + tAHW) - 15$	16.25	OK
Write signal valid time	tWSW	170		tDSTRDWR + tWRDWR	$TCYK * (1/2 + tAHW) - 15 + TCYK * (1 + n) - 15$	188.75	OK

READ

Item	Symbol	MIN.	MAX.	Corresponding Time	Calculation	Result	Evaluation
Cycle time	tCYCLE	312	---	---	$TCYK * (3 + tASW + tAHW + n + i)$	375	OK
ALE width	tALEW	10	---	tWSTH	$TCYK * (1 + i + tASW) - 15$	110	OK
Address setup time	tAADS	11	---	tSAST	$TCYK * (1/2 + tASW) - 20$	73.75	OK
Address hold time	tAADH		---	tHSTA	$TCYK * (1/2 + tAHW) - 15$	16.25	OK
Read data disable time	tRADH	8	---	tHRDID	0	0	OK
Read signal delay time	tARD	---	50	tDSTRDWR	$TCYK * (1/2 + tAHW) - 15$	16.25	OK
Read data delay time (RD)	tRAD	---	130	tSRID	$TCYK * (1 + n) - 25$	162.5	OK

READY

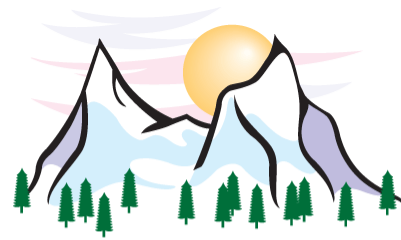
Item	Symbol	MIN.	MAX.	Corresponding Time	Calculation	Result	Evaluation
RDY signal delay	tWTD	---	105	tSSTWT1	$TCYK * (1 + tAHW) - 25$	37.5	OK
RDY signal width	tWTW	---	140	tHSTWT1 - tSSTT1	$TCYK * (n + tAHW) - TCYK * (1 + tAHW) + 25$	87.5	OK

Examples of TF542NG-compatible MPUs

Manufacturer	Model	Read operation	Write operation	RDY operation	Usage Conditions
Fujitsu	MB90F568TPFM*	OK	OK	OK	"Software wait = 3" or "Software wait = 2 + hardware wait"
NEC	uPD70F3716GC-8EA**	OK	OK	OK	"Address setup wait = 1 + Software data wait = 2"

*OMRON uses this CPU in its products

** Theoretical calculation only.



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MPU I/F in TF557NF ASIC for Slaves

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Overview of TF557NF

- ASIC for MPUs with 8-bit/16-bit external data bus
- Equipped with 4 general I/O ports

ASIC Interface Functions and Remarks

- Reads from/writes to registers and buffer area according to Read/Write control signal and address/data signals from MPU.
- Supports MPU with multiplex buses.
- Hardware wait output by RDY signal.
- Bus access, software wait, and hardware wait in MPU must be set in consistency with the ASIC requirements for bus cycle and AC timing.
- Full-decode of 16 address signals 0 to 15.
- Notifies frame transmission/reception on CompoNet network to MPU by outputting external interrupt using INT signal.
- Supports 8-bit or 16-bit data bus, according to the mode setting for MPU data bus. Once reset, it operates in 16-bit mode. When connecting to an 8-bit MPU, be sure to set MPU data bus mode to 8-bit data bus.

<In 16-bit mode>

Interfaces to MPU through 16-bit wide data bus, allowing word-unit or byte-unit access.

<In 8-bit mode>

Interfaces to MPU through 8-bit wide data bus, allowing byte-unit access.

Note: "Word-unit and byte-unit access" signifies accessing data width under a given hardware constitution. It does not represent software data type.

TF557NF Interface

Pins

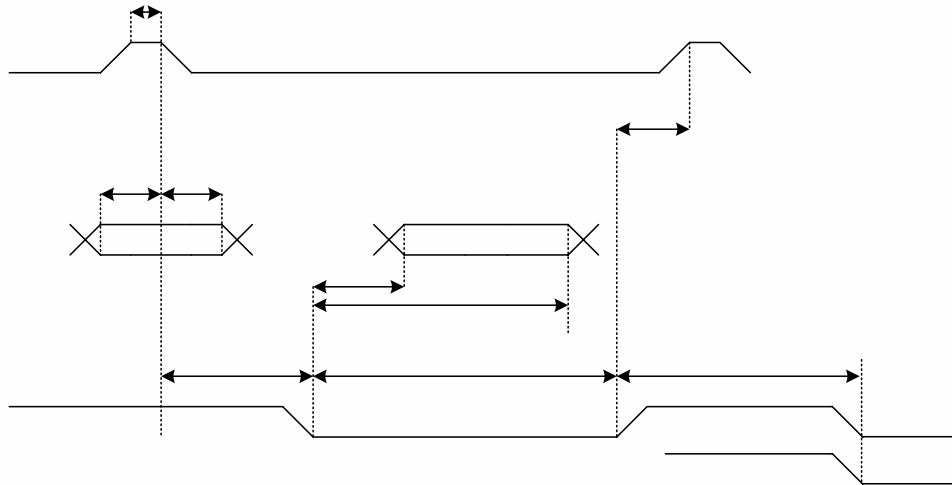
Pin Name	I/O	Description	True Value
WRHZ	IN	Write control of data bus upper 8 bits	L
WRLZ	IN	Write control of data bus lower 8 bits	L
RDZ	IN	Read control	L
ALE	IN	Address latch enable	H
AD15 to AD0	I/O	Address data bus	---
INT0Z	OUT	Interrupt	L
RDY	OUT	Hardware wait	L

Address Area

Byte Address	Area Name
2000h 20E3h	Registers
	Reserved (Data unspecified)
2100h 211Fh	INBuffer
2120h 213Fh	OUTBuffer
	Reserved (Data unspecified)
2160h 2191h	EventSendBuffer
	Reserved (Data unspecified)
21A0h 21D1h	EventReceiveBuffer
	Reserved (Data unspecified)

Attention: The ASIC address must be mapped to the area starting from xxx2000hex!

AC Timing of TF557NF: WRITE



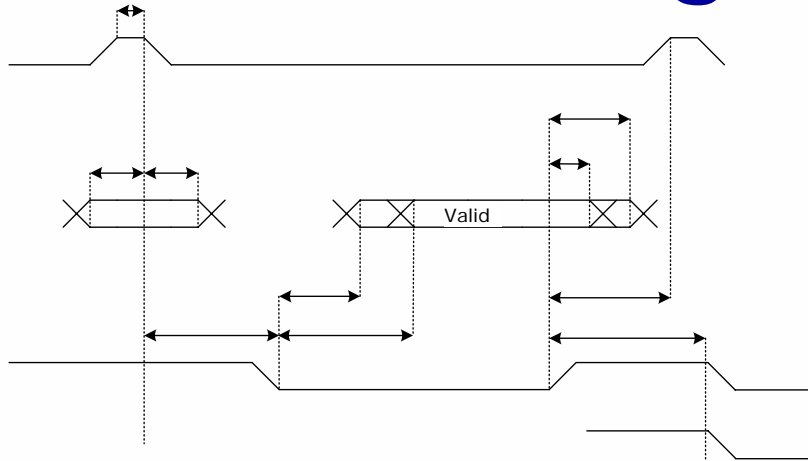
(VDD = 3.3 ±0.3V, TA = -40 to 85°C, CL = 15pF)

(unit: ns)

ALE

Item	Mark	MIN.	MAX.
ALE pulse width 1	(1)	7	---
Valid address to ALE ↓	(2)	10	---
Address valid time from ALE ↓	(3)	12	---
ALE ↓ to WR ↓	(4)	0	---
WR ↓ to Start of valid data	(5)	---	52.13
WR ↓ to End of valid data	(6)	113.84	---
WR pulse width	(7)	177.37	---
WR ↑ to ALE ↑	(8)	0	---
WR ↑ to WR/RD ↓	(9)	31.26	---

AC Timing of TF557NF: READ



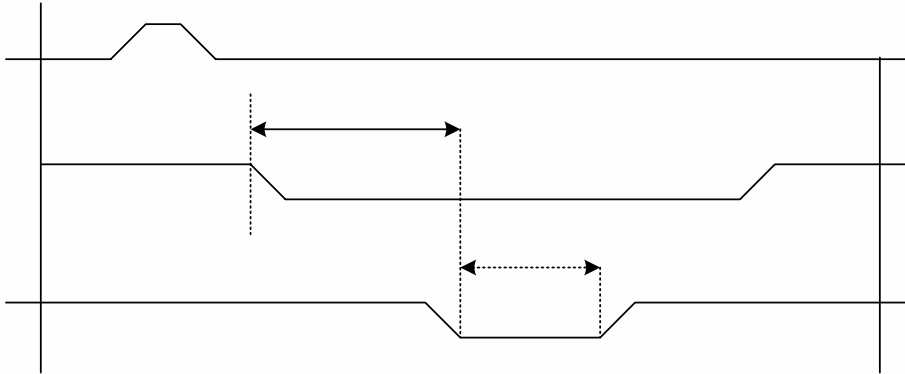
(VDD = 3.3 ±0.3V, TA = -40 to 85°C, CL = 15pF)

(unit: ns)

ALE

Item	Mark	MIN.	MAX.
ALE pulse width ^①	(1)	7	---
Valid address to ALE ↓	(2)	10	---
Address valid time from ALE ↓	(3)	12	---
ALE ↓ to RD ↓	(4)	0	---
RD ↓ to data output	(5)	52.87	---
RD ↓ to valid data output	(6)	---	168.17
Valid data hold time from RD ↑	(7)	---	1
Data hold time from RD ↑	(8)	12.05	---
RD ↑ to ALE ↑	(9)	0	---
RD ↑ to RD/WR* ^②	(10) ^③	31.26	---

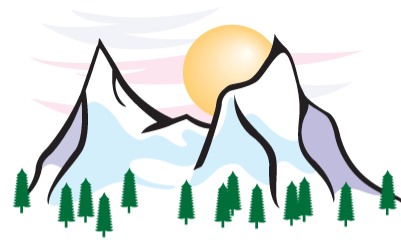
AC Timing of TF557NF: READY



(VDD = 3.3 ±0.3V, TA = -40 to 85°C, CL = 15pF) (unit: ns)

Item	Mark	MIN.	MAX.
RDZ/WR*Z ↓ to RDY ↓	(1)	63.62	---
RDY valid time	(2)	93.6	---

ALE



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A TF557NF Analysis Example (no guarantee of proper operation)

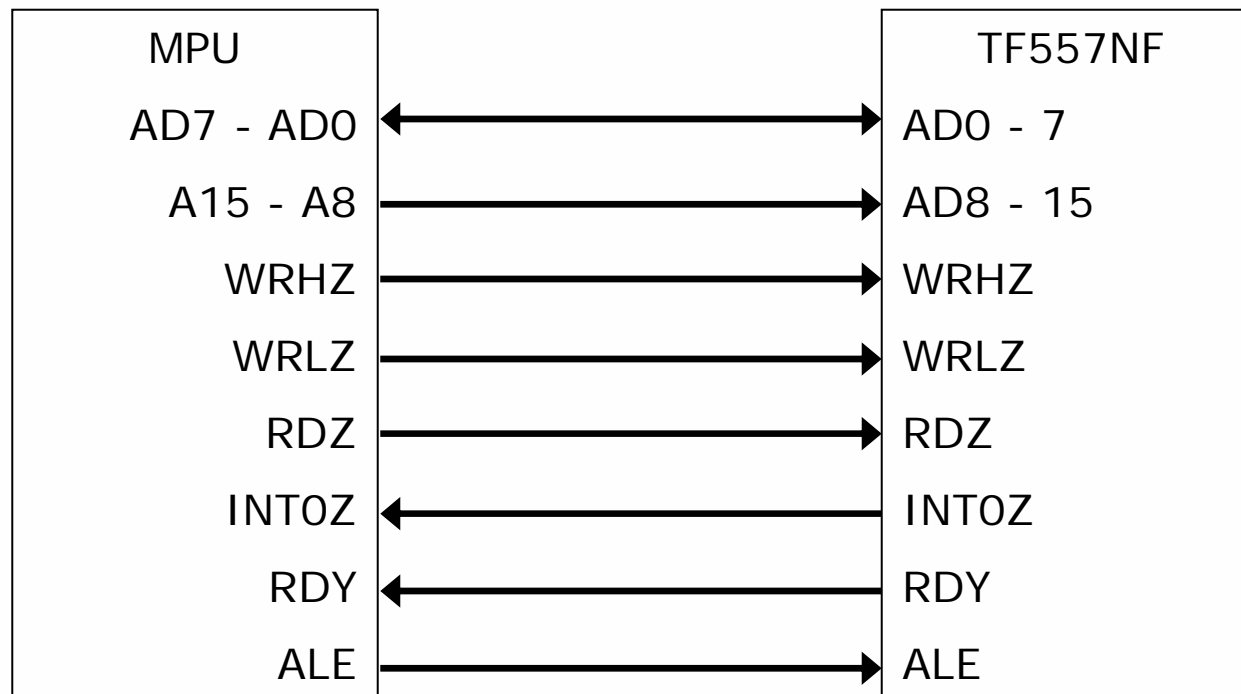
MPU manufactured by FUJITSU

Model: MB90F568TPFM

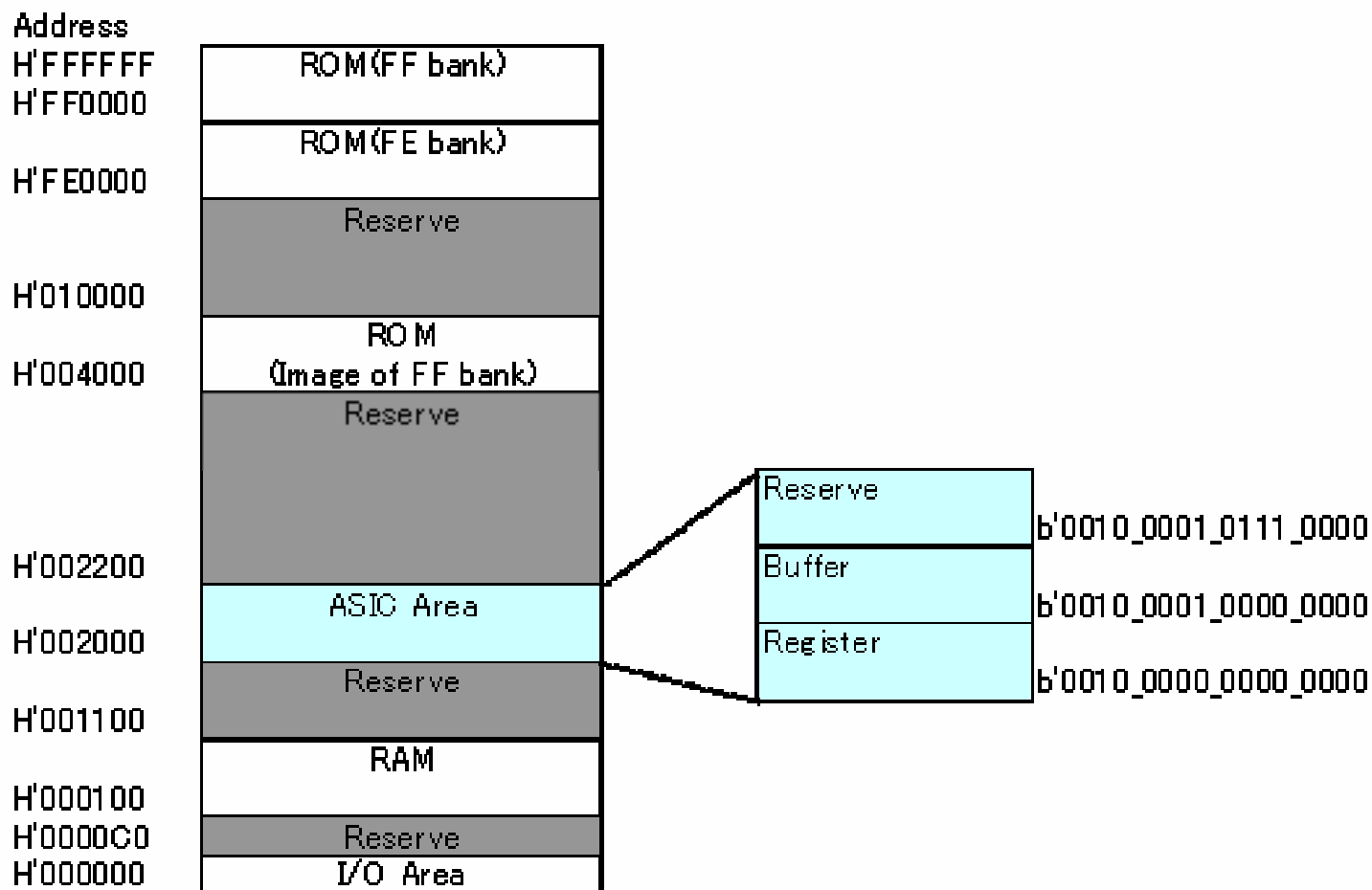
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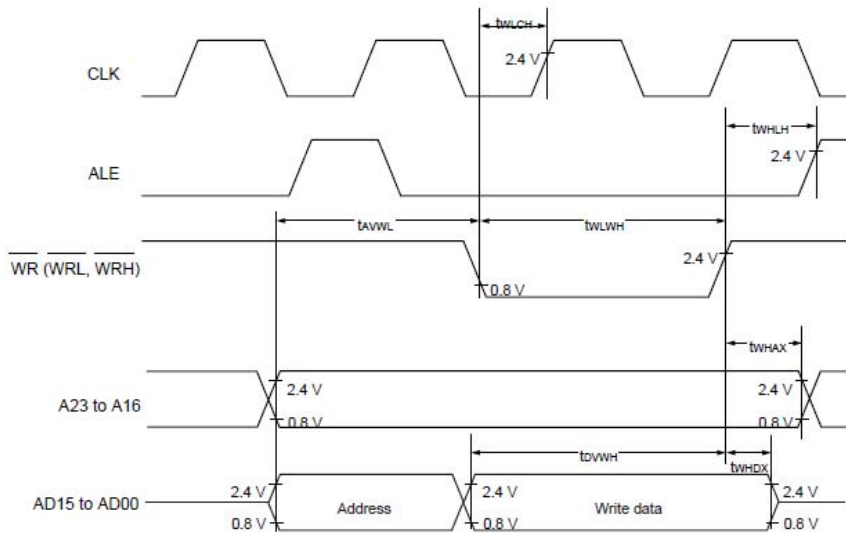
Connection Image: MB90F568TPFM and TF557NF



Memory Map: MB90F568TPFM



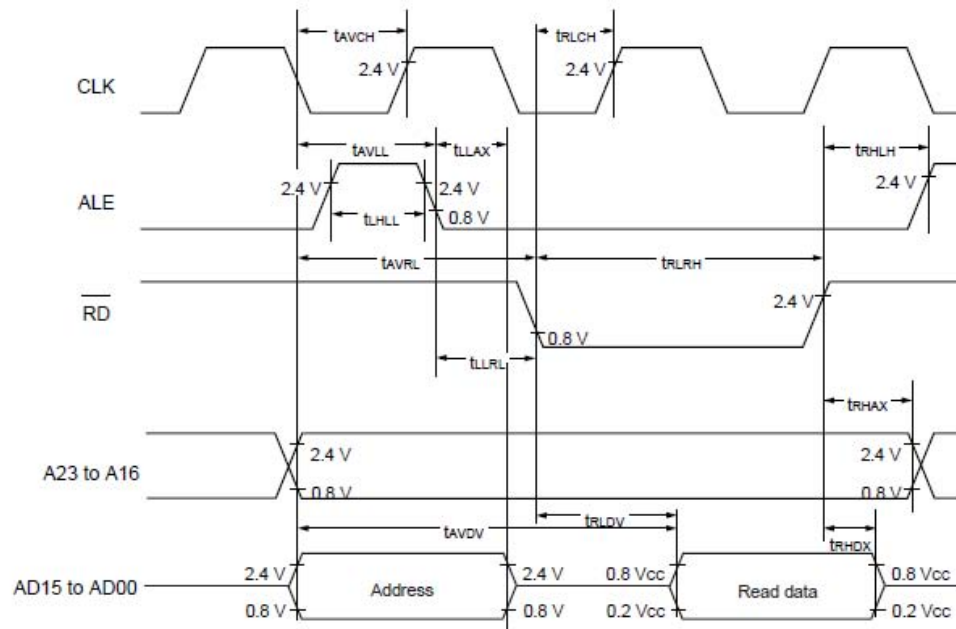
AC Timing of MB90F568TPFM: WRITE



($V_{cc} = 2.7$ to $3.6V$, $V_{ss} = AV_{ss} = 0V$, $T_A = -40$ to $+85^{\circ}C$) (unit: ns)

Item	Symbol	MIN.	MAX.
Valid Address to WR ↓	tAVWL	tCP-15	---
WR pulse width	tWLWH	3tCP/2-20	---
Valid data output to WR ↑	tDVWH	3tCP/2-20	---
Data hold time from WR ↑	tWHDX	20	---
Address valid time from WR ↑	tWHAX	tCP/2-10	---
WR ↑ to ALE ↑	tWHLH	tCP/2-15	---
WR ↑ to CLK ↑	tWLCH	tCP/2-20	---

AC Timing of MB90F568TPFM: READ



($V_{cc} = 2.7$ to $3.6V$, $V_{ss} = AV_{ss} = 0V$, $T_A = -40$ to $+85^{\circ}C$) (unit: ns)

Item	Symbol	MIN.	MAX.
ALE pulse width	tLHLL	tCP/2-20	---
Valid address to ALE ↓	tAVLL	tCP/2-20	---
Address valid time from ALE ↓	tLLAX	tCP/2-15	---
Valid address to RD ↓	tAVHL	tCP-15	---
Valid address to Valid data input	tAVCV		5tCP/2-60
RD pulse width	tRLRH	3tCP/2-20	---
RD ↓ to valid data input	tRLDV	---	3tCP/2-60
Data hold time from RD ↑	tRHDX	0	
RD ↓ to ALE ↑	tRHLH	tCP/2-15	
Address valid time from RD ↑	tRHAX	tCP/2-10	
Valid address to CLK ↑	tRLCH	tCP/2-20	
RD ↓ to CLK ↑	tRLCH	tCP/2-20	
ALE ↓ to RD ↓	tLLRL	tCP/2-15	

Timing Verification Results MB90F568TPFM and TF557NF

WRITE

ASIC Requirements				Verification for Fujitsu MPU		
Item	Mark	MIN.	MAX.	Corresponding Time	Calculation	Evaluation
ALE pulse width	(1)	7	---	tLHLL	$tCP/2-20 = 11.25$	OK
Valid address to ALE ↓	(2)	10	---	tAVLL	$tCP/2-20 = 11.25$	OK
Address valid time from ALE ↓	(3)	12	---	tLLAX	$tCP/2-15 = 16.25$	OK
ALE ↓ to WR ↓	(4)	0	---	tLLRL	$tCP/2-15 = 16.25$	OK
WR ↓ to Start of valid data	(5)	---	52.13	---	---	OK
WR ↓ to End of valid data	(6)	113.84	---	$tDVWH + tWHDX + 3 \text{ wait}$	$(3tCP/2-20) + (3tCP) = 156.25$	OK
WR pulse width	(7)	177.37	---	$tWLWH + 3 \text{ wait}$	$(3tCP/2-20) + (3tCP) = 261.25$	OK
WR ↑ to ALE ↑	(8)	0	---	tWHLH	$tCP/2-15 = 16.25$	OK
WR ↑ to WR/RD ↓	(9)	31.26	---	$tWHLH + tLHLL + tLLRL$	$(tCP/2-15) + (tCP/2-20) + (tCP/2-15) = 43.75$	OK

READ

Item	Mark	MIN.	MAX.	Corresponding Time	Calculation	Evaluation
ALE pulse width	(1)	7	---	tLHLL	$tCP/2-20 = 11.25$	OK
Valid address to ALE ↓	(2)	10	---	tAVLL	$tCP/2-20 = 11.25$	OK
Address valid time from ALE ↓	(3)	12	---	tLLAX	$tCP/2-15 = 16.25$	OK
ALE ↓ to RD ↓	(4)	0	---	tLLRL	$tCP/2-15 = 16.25$	OK
RD ↓ to data output	(5)	52.87	---	$tLLRL - tLLAX$	$(tCP/2-15) - (tCP/2-15) = 0$	OK
RD ↓ to valid data output	(6)	---	163.7	$tRLDV + 3 \text{ wait}$	$(3tCP/2-60) + (3tCP) = 221.25$	OK
Valid data hold time from RD ↑	(7)	---	1	tRHDX	0	OK
Data hold time from RD ↑	(8)	0.95	---	tRHDX	0	OK
RD ↑ to ALE ↑	(9)	0	---	tRHLH	$= 16.25$	OK
RD ↑ to RD/WR*Z ↓	(10)	31.26	---	$tRHLH + tLHLL + tLLRL$	$(tCP/2-15) + (tCP/2-20) + (tCP/2-15) = 43.75$	OK

READY

Item	Mark	MIN.	MAX.	Corresponding Time	Calculation	Evaluation
RDZ/WR*Z ↓ to RDY ↓	(1)	63.62	---	$tWLCH - tRYHS + 2 \text{ wait}$ $(tRLCH - tRYHS + 2 \text{ wait})$	$(tCP/2-20) - 45 + 2tCP = 11.25$	OK
RDY valid time	(2)	93.6	---	$tRYHS + tRYHH + 2 \text{ wait}$	$45 + 0 + 2tCP = 170$	OK



TF557NF-compatible MPUs

Manufacturer	Model	Read operation	Write operation	RDY operation	Usage Conditions
Fujitsu	MB90F568TPFM*	OK	OK	OK	"Software wait = 3" or "Software wait = 2 + hardware wait"
NEC	uPD703015BGC- 8 EU **	OK	OK	OK	"Software wait = 3" or "Software wait = 2 + hardware wait"
Atmel	AT89LS52-16AU**	OK	OK	---	Operating frequency: 15 MHz max.
Atmel	AT89C51RB2-RLTUL **	OK	OK	---	Operating frequency: 25 MHz max. Standard Clock
Atmel	AT89C51RC2-RLTUL **	OK	OK	---	Operating frequency: 25 MHz max. Standard Clock
Atmel	AT89C51ED2-RLTUL **	OK	OK	---	Operating frequency: 25 MHz max. Standard Clock

*OMRON uses this CPU in its products

** Theoretical calculation only.